REMARKS

Claims 1, 10, 11, 21 and 24-30 and 33-41 are pending in this application upon entry of this amendment. Claim 40 is added, claims 31-32 is canceled, and claims 1, 11, 21, 24 33-35 and 37-38 are amended. New claim 40 is supported by the paragraph [0092] of the specification. Amendments to claims 1 and 11 are supported by canceled claims 31 and 32 and paragraphs [0069] and [0082] of the specification.

Claims 1, 10, 11, 21 and 24-40 stand rejected under 35 USC 103(a) on Fukunaga (U.S. Patent Publication No. 2002/0044584) in view of Yoshida (U.S. Patent Publication No. 2002/0041613). Applicants respectfully traverse this rejection.

Claim 1 recites "the quantum well active layer and the upper guide layer are doped with a second conductivity type of impurity." Neither Fukunaga nor Yoshida discloses or suggests both the quantum well active layer and the upper guide layer having a second conductivity type of impurity. Specifically, the upper guide layer 63 of Fukunaga is doped with p-type material while the active layer 55 is undoped. See Fukunaga, paragraph [0055]. Also, the active layer 4 of Yoshida is doped with p-type material while the upper guide layer 3B is undoped. See Yoshida, paragraph [0003]. However, in neither of the references are both the well active layer and the upper guide layer doped using the same conductivity type of impurity.

The Office Action asserts that it would have been obvious to one of ordinary skill in the art to dope the active layer 55 of Fukunaga's device with p-type material to reduce the series resistance and thermal impedance of the device. Applicants respectfully disagree. The inventors of Yoshida discovered that doping the active layer 4 with impurities, in that particular structure, helps reduces device resistance and thermal impedance of the device. In Yoshida, the active layer 4 is sandwiched between two confinement layers 3A and 3B, which arguably correspond to the guide layers of Fukunaga. The confinement layers 3A and 3B of Yoshida are both undoped, which likely contribute to high device resistance. In Fukunaga, however, the active layer 55 of Fukunaga, and

the surrounding tensile strain barrier layers 54, 56, are sandwiched by a lower n-type waveguide layer 53 and an upper p-type waveguide layer 57. There is no evidence that Fukunaga's device suffers from the same limitations (i.e., high resistance and thermal impedance) that Yoshida is attempting to solve. In particular, since the doped waveguide layers 57 of Fukunaga are doped, it is likely that Fukunaga does not undergo high resistance and thermal impedance as does Yoshida. Further, there is no evidence doping the active layer in Fukunaga's device would produce similar results as Yoshida. Thus, one of ordinary skill in the art would not have been motivated to dope the active layer 55 in the device of Fukunaga with impurities. In this invention, the arrangement of quantum well active layer and the upper guide layer both being doped with a second conductivity type of impurity suppresses the diffusion of the impurity from the upper clad layer. See paragraph [0069] of the application. Accordingly, claim 1 is allowable over the cited references.

Claims 11, 21 and 24 recite similar features as claim 1 and are allowable for the same reasons. Claims 10, 20, 29, 30, 33-41 depend variously from claims 1, 11, 21 or 24 and are allowable for the same reasons.

Claim 25 recites "the quantum well active layer is grown while being doped with Si as a first conductivity type of impurity." Claim 27 recites "the quantum well active layer is grown while being doped with Zn as a second conductivity type of impurity." These features are not taught by either Fukunaga or Yoshida. The Examiner provides no evidence or reason why incorporation these features into the combination of Fukunaga and Yoshida would be have been obvious to one of ordinary skill in the art. Accordingly, claims 25 and 27 are allowable. Claims 26 and 28 depend from claims 25 and 27, respectively, and are similarly allowable.

In view of the above, each of the claims in this application is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone

conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief, including extensions of time, and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **204552030500**.

Dated: June 16, 2008

Respectfully submitted,

By _____

Amir R. Rohani
Registration No. 61,782
MORRISON & FOERSTER LLP
1650 Tysons Blvd, Suite 400
McLean, Virginia 22102
(703) 760-7757